REMARKS

Claims 1-26 are pending. Applicants respectfully request reconsideration and allowance of this application in view of the following remarks.

Claims 1-26 are again rejected under 35 U.S.C. 103(a) over Eto in view of APA. This rejection is respectfully traversed.

The present invention as recited in claim 1 overcomes the deficiencies of the combination of Eto and APA for reasons already discussed in detail on pages 7-8 of the Remarks in the Amendment filed on February 7, 2004.

As recited generally in claims 1 and 11, when the control signal *Sa* changes from the H-level to the L-level, the change causes, *inter alia*, only the high-side transistor T11 to turn on to therefore provide a charging current from the power supply line 16 through the transistor T11 and the resistor R11 and the output terminal 13 to the gate capacitors of the MOSFET 14. This causes the output voltage V_o to rise rapidly to thereby turn on the MOSFET 14 once V_o exceeds a voltage threshold V_{TH} (page 14, lines 11-19). The high-side transistor T11 is then turned off again in addition to the high-side transistor T12.

As recited generally in claims 6 and 11, when the control signal *Sa* changes from the L-level to the H-level, the change causes, *inter alia*, only the low-side transistor T12 to turn on, and the drive circuit 11 to discharge the charge on gate capacitors of the MOSFET 14 to the ground line 17 through the output terminal 13 and the transistor 12 to thereby rapidly decrease V_o. The low-side transistor T12 is then turned off again in addition to the high-side transistor T11 when V_o falls below a level indicated by Equation (4) on page 16 of the specification (page 14, line 20 – page 16, line 18).

By maintaining both transistors T11 and T12 in an off state at all times other than switching between the H-level and the L-level, i.e., when the circuit is in steady state operation,

the present invention decreases power consumption by amounts consumed by the transistors T11 and T12 (page 27, lines 8-13 and FIG. 2).

However, in both Eto and APA, at least one of a high-side transistor and a low-side transistor is on at all times. Therefore, neither of the circuits disclosed in the references has the power-saving capability of the present invention. (See, e.g., page 3, line 26 – page 4, line 15 of the present application and page 8, lines 3-10 of the Remarks in the February 3, 2004 Amendment.) Unlike the circuit in Eto, which as discussed in the previous Amendment operates to compare a reference voltage V_{ref} to an output voltage V_{pr} and to bring the voltages into agreement to provide a stable output voltage V_{pr}, the circuit of the present invention does not compare the input voltage *Sa* and the output voltage V_o, and does not operate to bring the two voltages into agreement. Rather, the circuit of the present invention operates to drive the switching element (MOSFET 14).

Further regarding Eto, Applicants respectfully question the procedural validity of using this reference for a 103(a) rejection, as it is not analogous to the present invention. In order for the Examiner to rely on a reference as a basis for an obvious rejection, the reference must be analogous to the applicant's invention. The reference is analogous if it is in the field of applicant's endeavor or, if not, is reasonably pertinent to the particular problem with which the inventor was concerned. (See *In re Oetiker*, 977 F.2d 1443, 1446 (Fed. Cir. 1992), MPEP 2141.01(a) Rev. 1, Feb. 2000.)

Eto and the present invention are in different fields of endeavor. For example, the circuit in Eto is an integrated circuit (IC) including a DRAM for use in microcomputers and having an operating range of 0-5V. The circuit of the present invention is an analog circuit for use in, for example, a power circuit, and may have an operating range of, for example, 0-35V. Therefore, reducing power consumption is more problematic in the drive circuit of the present invention

compared to the lower power circuit of Eto. One skilled in the art would have no motivation to look to the IC in Eto for producing a stable output voltage of 0-5V in combination with the deficient teachings of APA to produce the drive circuit with the reduced power consumption capability of the present invention.

Further evidence that Eto is nonanalogous art is evidenced by the fact that Eto appears to be classified differently than the present invention. Specifically, the present invention has been preliminarily classified in class 361, while Eto is classified in class/subclass 323/313, and classes 323, 330 and 327 were searched during examination thereof. "Patent Office classification of references and...the official search notes are some evidence of nonanaology or analogy." (See MPEP 2141.01(a) Rev. 1, Feb. 2003.)

Therefore, because Eto is a nonanalogous reference, and is directed to providing a solution (stable output voltage) that is completely different from that of the present invention, it is respectfully requested that the rejection of claims 1-26 in view of Eto and APA under 35 U.S.C. 103(a) be withdrawn.

Regarding the Examiner's comments in the Response to Arguments section on page 4 of the present Final Rejection, the Examiner asserts that "the features upon which the applicant relies (i.e. a power consumption reduction aspect of the detecting circuit) are not recited in the rejected claim(s)." Applicants assert that the features recited in the present claims distinguish the present invention over the cited art as-is. Specifically, when for example the control signal Sa changes from the L-level to the H-level when the MOSFET 14 is switched from the on-state to the off-state, the high-side transistor T11 remains off, and the low-side transistor T12 is turned on until the MOSFET 14 switches to the off-state, and is thereafter turned off. This feature distinguishes the present invention from the cited references, in which at least one of high and low side transistors remains on at all times.

In view of the foregoing, the Applicants respectfully submit that this application is in condition for allowance. A timely notice to that effect is respectfully requested. If questions relating to patentability remain, the Examiner is invited to contact the undersigned by telephone.

Please charge any unforeseen fees that may be due to Deposit Account No. 50-1147.

Respectfully submitted,

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